Computer Simulation of ESD and Lightning Events

Douglas C. Smith
D. C. Smith Consultants
P. O. Box 1457, Los Gatos, CA 95031
Tel: 800-323-3956
Email: doug@dsmith.org
Web: http://www.dsmith.org

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Douglas C. Smith
AT&T Information Systems
Middletown, NJ 07748
201-957-5008

Abstract

Predicting effects of ESD and lightning on the operation of electronic circuits is difficult for many reasons. Among the problems encountered in the measurement of ESD and lightning effects are difficulty of instrumentation and lack of a controlled environment for testing. This paper explores computer simulation techniques that have been used with success to predict circuit response to ESD and lightning events.

Introduction

Accurate modeling of equipment and environment is a necessary base for useful simulations of lightning and ESD events. Most of the modeling effort must be put into system level modeling for accurate predictions at the device level.

Modeling techniques for electronic equipment are similar for both lightning and ESD events. Modeling of the ESD event itself is more difficult than for lightning, however, requiring sophisticated features in the circuit analysis program.

In this paper, I compare modeling techniques for both lightning and ESD events and relate these to system level modeling. Finally, I present computer simulation results for these two stresses and discuss limitations of the simulations and conclusions that can be drawn from them. All computer simulations for this paper use ADVICE, a SPICE-like circuit analysis program written at AT&T Bell Laboratories in Murray Hill, New Jersey[1]. ADVICE is used extensively within AT&T.

Modeling - General

Lightning Events

In general, modeling of lightning events is simpler than ESD events for several reasons. There exist models for three common types of lightning surges that electronic equipment is normally exposed to. Part 68 of the Federal Communications Commission Rules spells out characteristics of lightning surges that occur on telephone connections and power line connections that PBX equipment is likely to endure.

The three FCC surges are as follows. A metallic voltage surge (applied differentially to the wire pair) is defined as having a 10 microsecond maximum risetime to a peak of 800 volts and a 560 microsecond minimum decay time to half crest with a minimum peak current of 100 Amperes available. A longitudinal voltage surge (applied common mode to the wire pair) is defined as having a 10 microsecond maximum risetime to a peak of 1500 volts and a 160 microsecond minimum decay time to half crest. The minimum peak current available is 200 Amperes. Finally, a power line surge is defined as having a 2 microsecond maximum risetime to a peak of 2500 volts and a 10 microsecond minimum decay time to half crest applied between the phase and neutral terminals of the AC power line. The minimum peak current available from this surge is 1000 Amperes.

Notice that the time scales of the above surges are in microseconds. Compared to an ESD event these relatively slow waveforms of the lightning surges simplify the modeling problem considerably.

Ground potential differences between pieces of equipment can also occur during lightning hits. These surges are not as well defined because of the many possible geometries and absence of protectors such as the carbon blocks used on telephone connections. Luckily, equipment design, at least in the telephone industry, is adequately protected by designing for the three well defined surges mentioned above. For this paper I will address only effects of these three surges.

ESD Events

Simulation of ESD events is similar to that of lightning events except for several factors that make the process more difficult[2]. As mentioned above, the time scales for lightning events is measured in microseconds. For most ESD events the need to account for much higher frequency components, as a result of subnanosecond risetimes, can significantly increase the effort required for accurate simulation results. For example, transmission line models are needed more often in ESD simulation than in lightning simulation.

Modeling of the electrostatic discharge itself is also more complicated because of the lack of standard specifications on ESD generators. One approach that I have used is to simulate the circuit of one commercial ESD generator. The circuit appears in Figure 1 below.

The circuit consists of a 150pF storage capacitor with a 150 Ohm series resistance and an ideal switch. The ideal switch simulates the fast risetime of a spark and its ability to leave charge on the capacitor. It also disconnects the generator from the circuit when the spark is extinguished. The ADVICE description of the circuit appears in Table 1 below. Resistors and capacitors (r/c as first letter) are each described on one line by the element name, the two connection nodes, and by the element value in that order. An ideal switch is specified as "s1." It is connected between nodes "gen" and "g2" and is controlled by the voltage between nodes "g3" and ground (gnd). It is closed when the voltage on the

storage capacitor has exceeded 2kV and is still above 1kV. The switch opens 5 nanoseconds after the capacitor voltage drops below 1kV.

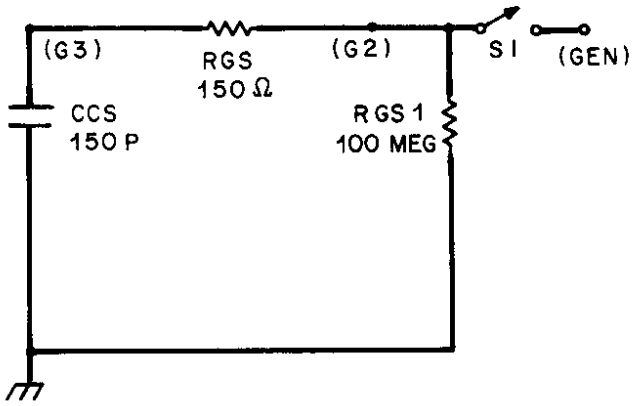


Figure 1

Table 1
Simulated ESD Generator

```
rgs  g2  g3  150
rgs1 g2  gnd 100meg
ccs  g3  gnd 150pF
s1 gen g2 g3 gnd ideal(2kv 1kv 5ns) off
```

Rgs1 is needed to complete a DC path to ground when the switch is open. It also simulates real leakage paths. The 15 millisecond time constant with the 150 pF charge storage capacitor does not affect the simulation which typically runs only for a few microseconds.

The use of s1 complicates the choice of timesteps and convergence parameters in ADVICE. I will discuss this later.

Results obtained using this generator have correlated well with those using the equivalent ESD generator in the lab.

System Level Modeling

Lightning

Most of the parameters that are important to modeling the lightning event are considered parasitics to normal operation. For instance, the 20nH per inch inductance of a ground wire can present appreciable impedance over a 10 foot wire with microsecond risetimes. Capacitance between the equipment being modeled and its surroundings can become significant and cause unwanted resonances with wire inductances.

Capacitance values are more significant than one might expect because of the high voltages and frequencies encountered. Consider the capacitance of two adjacent equipment cabinets with a 1 centimeter spacing and facing surfaces having 2 square meters of surface area. The capacitance of a parallel plate capacitor is:

$$C = Eo*A/D$$

where A is the area of the plates, D is the spacing, and Eo is 8.85x10**(-12) in free space. For the case being considered the capacitance of the adjacent cabinets is about 1800 pF.

Consider, Figure 2, the case of 2 adjacent cabinets each connected to ground individually with 10 foot ground wires.

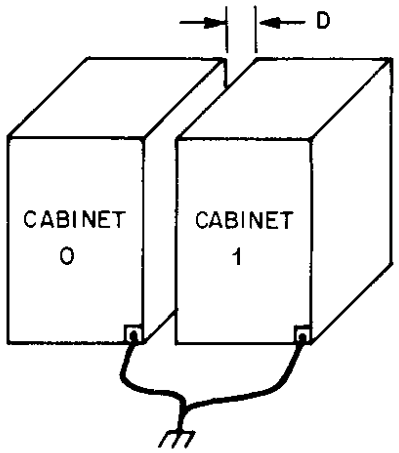


Figure 2

Using 20nH/in for the inductance of the ground wires and 1800pF for the cabinet to cabinet capacitance, the equivalent circuit of Figure 3 results.

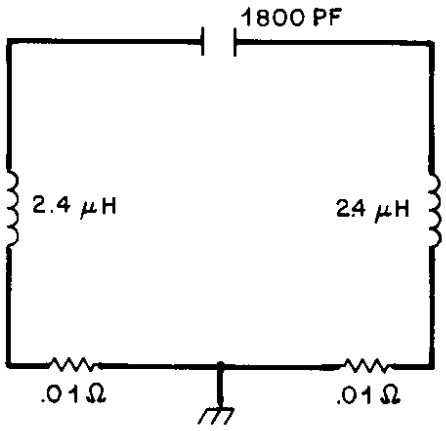


Figure 3

The circuit of Figure 3 resonates near 1.7 MHZ. With variations in cabinet spacing, mutual inductance between the ground wires, and wire length, this resonance can occur in the frequency range where the lightning surge has significant energy.

In general, large electronic systems, such as PBX's and mainframe computers, may require many cabinets in a large equipment room. Figure 4, on the next page, depicts a 5 cabinet PBX system with ground wires connecting each cabinet to a single point ground and its equivalent circuit.

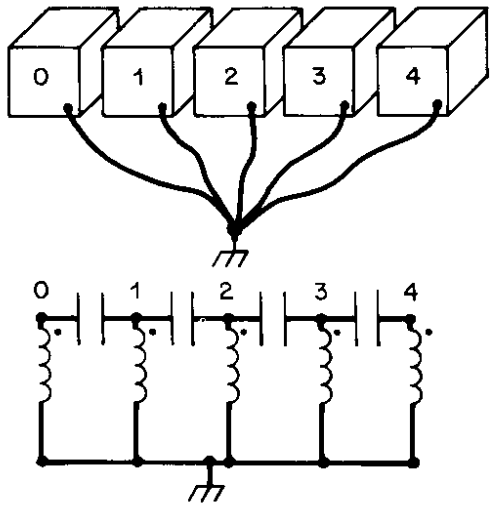


Figure 4

To understand the importance of these coupled tuned circuits we must consider in the system model at least a simplified version of the circuits contained in the cabinets. In many systems the cabinets contain shelves of circuit cards plugged into a backplane that has a layer of signal ground. In some cases signal ground is connected to the grounded cabinet directly and in other cases is returned to building ground through a separate wire from the cabinet.

Figures 5 and 6 show cabinets with isolated backplanes and backplanes connected to the cabinet respectively.

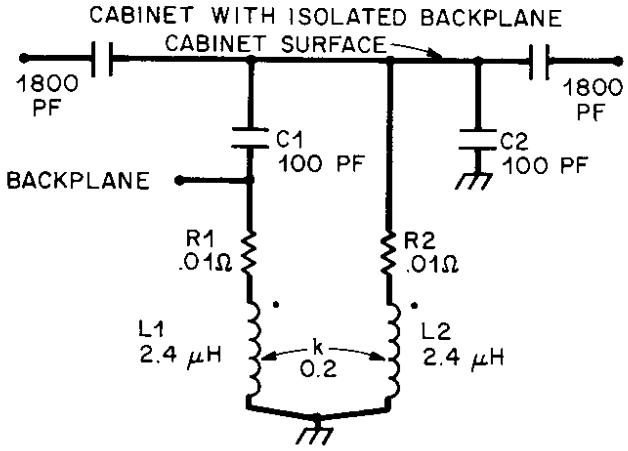


Figure 5

In these two figures, C1 represents the backplane to cabinet capacitance. The value of 100 pF represents a reasonable estimate of a typical value. C2 represents the cabinet to nearby ground and free space capacitance. Again, this is an estimate of an expected typical value. Remember that these parameters in the models can vary by a factor of 10 depending on the particular situation.

R1 and R2 in Figures 5 and 6 represent the ground wire resistances and L1 and L2 represent the inductances of the ground wires having lengths of 10 feet. R3 and L3 in Figure 6 model the connection of the backplane to the cabinet.

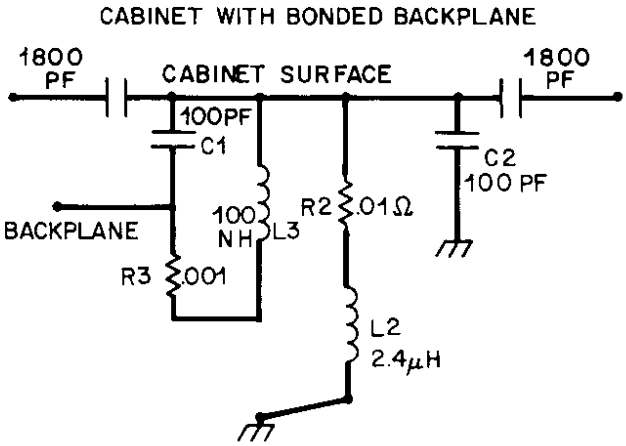


Figure 6

Although these models are coarse they are valid up to a few MHZ for large systems. This frequency range is enough to account for most of the lightning energy normally encountered.

For a telephone system, lightning surges incoming on the talking pairs of wires may be routed into the backplane through current limiting resistors on the order of 100 ohms. If multicabinet systems, composed of units shown in Figures 5 or 6, are connected in a computer simulation, intercabinet and cabinet to ground voltages and their effect on circuitry internal to the cabinets can be predicted. Some surprising results are discussed later in this paper.

Electrostatic Discharge

Modeling of the ESD event on a system level is more difficult, mainly because of higher frequency components and modeling of the spark itself.

To maintain accuracy with the higher frequency components of the energy source, models of circuits and interconnections become much more complicated. For instance, transmission line effects must be accounted for in cables of only a foot or two in length.

Transmission line modeling can be complicated in that some circuits may not fit nicely into the transmission line model supplied in a circuit analysis program. This can be handled by modeling the line as a series of lumped element representations. Each lumped element circuit must represent a length of the circuit that has a time delay small compared to the risetime of any wavefronts that pass through it. It is almost required that the circuit analysis program used, such as ADVICE, have a nested subcircuit capability. Without using nested subcircuits a 100 foot cable using 3 inch lumped models would require 400 lumped element segments. This is 1000 or more elements that need to be typed into the simulation code.

When subcircuits are used, the lumped element segment is defined as a subcircuit and then several of these may be used to define a subcircuit to represent one foot of the cable or circuit. Ten of these subcircuits are used to define a 10 foot segment and 10 of

these can be used to define a 100 foot segment. All this nesting of lumped element subcircuits generates thousands of components that the circuit analysis program needs to handle. However, the person running the simulation rarely needs to think about these thousands of components, just the endpoints of the circuit. The nesting of subcircuits keeps the size of the simulation code to a manageable level.

An example of this process appears below for a 10 foot section of coax cable. In the example resistors, capacitors, and inductors (r, c, and l as first letter) are each described on one line by the element name, the two connection nodes, and by the element value in that order. The element kcs is a coefficient of coupling between the two inductors specified. This has been set to .99999 and the part of the conductor inductances that are uncoupled are entered as discrete inductors lc2 and ls2. Lc2 and ls2 could have been eliminated and kcs lowered to its real value, but keeping the "leakage" inductances separate allows for easier inspection of the code. Elements starting with "x" contain the subcircuit specified as the last field on the line and connect to external nodes in the same order as specified in the subcircuit definition.

10 Feet Of Coax Cable

```
_subckt coax (ci,si,co,so)
*       3 inches of coax      *
rc      ci      cm1     0.0115
rs      si      sm1     0.0006
lc1     cm1     cm2     12.5nh
lc2     cm2     co      26.25nh
ls1     sm1     sm2     2.5nh
ls2     sm2     so      5.25nh
ccs     co      so      5.35pf
kcs     lc1     ls1     0.99999
_finis

_subckt coax1ft (ci,si,co,so)
*       1 foot of coax        *
xcoax1 ci  si  co1 so1 coax
xcoax2 co1 so1 co2 so2 coax
xcoax3 co2 so2 co3 so3 coax
xcoax4 co3 so3 co  so  coax
_finis

_subckt coax10ft (ci,si,co,so)
*       10 feet of coax       *
xcoaxf1  ci  si  co1 so1 coax1ft
xcoaxf2  co1 so1 co2 so2 coax1ft
xcoaxf3  co2 so2 co3 so3 coax1ft
xcoaxf4  co3 so3 co4 so4 coax1ft
xcoaxf5  co4 so4 co5 so5 coax1ft
xcoaxf6  co5 so5 co6 so6 coax1ft
xcoaxf7  co6 so6 co7 so7 coax1ft
xcoaxf8  co7 so7 co8 so8 coax1ft
xcoaxf9  co8 so8 co9 so9 coax1ft
xcoaxf10 co9 so9 co  so  coax1ft
_finis
```

This is a four terminal model for the coax cable. In ESD simulations it is necessary to use four terminal models for coax since the shield impedance must also be taken into account. Most circuit analysis programs that I have seen only have three terminal models available for transmission lines. The need for a four terminal model for coax cable is another example of the need for accurate high frequency models when simulating ESD effects on equipment.

Earlier I discussed modeling of the ESD spark. The way spark modeling is handled can result in convergence and/or accuracy problems in the simulation if care is not taken. For convenience Table 1 is repeated below. This is the ADVICE description of the ESD generator that appears in Figure 1.

Table 1
Simulated ESD Generator

```
rgs  g2  g3  150
rgs1 g2  gnd 100meg
ccs  g3  gnd 150pF
s1 gen g2 g3 gnd ideal(2kv 1kv 5ns) off
```

The problem is that the ideal switch generates a large voltage step on node "gen" between two timepoints. Many circuit analysis programs, and ADVICE in particular, are tailored to integrated circuit design (ADVICE is an acronym for "Aid in Design Verification for Integrated Circuit Engineering"). Because of the typically low voltages --5 to 10 volts-- encountered in IC design, the default convergence parameters in ADVICE are set correspondingly low. One of the default convergence parameters in ADVICE limits the allowable change in any node voltage between consecutive timepoints to 1.5 volts. When this parameter is violated, ADVICE reduces the timestep below the original specification in the simulation code until a) this condition is satisfied, or b) the timestep has been reduced by 9 orders of magnitude. In this way, ADVICE spends more CPU time when the voltages in the circuit are changing rapidly. This ensures accurate output with a minimum of CPU time used.

When using an ideal switch, as above, case "b" results. The timestep is effectively reduced to zero and the circuit will not converge. Thus, when s1 connects the capacitor ccs, charged to 15,000 volts, to the circuit, everything stops.

It is necessary to manually raise the consecutive timepoint threshold voltage above the expected voltage step. However, caution is required to maintain accurate output. Since the threshold needed is the initial voltage on ccs, it must be typically set to 10kV or more. Generally the point of running the simulation is to find out how much voltage is generated somewhere in the circuit. For solid state circuits one could be looking for relatively small voltages, certainly smaller than the required threshold voltage. A problem arises in that if the timestep is not set small enough for the rate voltages and currents are changing in all parts of the circuit, after the ESD event, errors will be generated. This is because the ability of the program to reduce the step size when voltages change too much in one timestep has been "disabled."

At first one is tempted to think of ways around this limitation. One possibility is to define the spark generator as a pulse generator with a very fast risetime, say one timestep. This does not work either because one must still define the one timestep threshold voltage to be enough to allow the generator to change that fast. The net result is that one is no better off than with the ideal switch and capacitor.

Solution of the problem lies in that the person running the simulation must make sure the timestep is set small enough to insure accuracy. This is easier than it sounds. First, the simulation is run with a timestep somewhat larger than is expected. Compare

the output plots with another simulation with the timestep set to one half of the original choice. Compare the results and keep running the simulations with the timestep set to one half of the previous run until two successive runs show no significant differences in waveshape or magnitudes in the time period common to both outputs. Later in this paper I will show an example of this procedure.

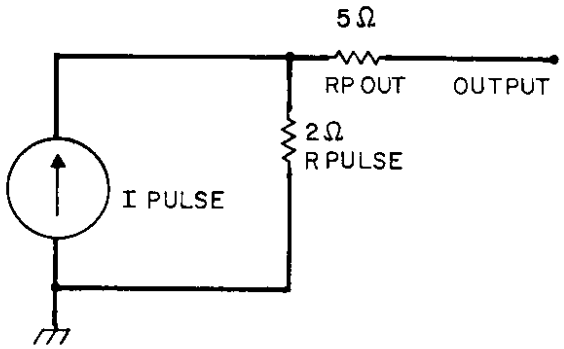
If the system to be simulated has a response to the ESD event that lasts for a long time, 10 microseconds or more, and has time constants of less than a nanosecond as well, the simulation could require a large amount of CPU time to run. An example I will present later requires timesteps of about 0.5 nanosecond and has response out to several microseconds.

Other system level parameters are modeled in a similar way to the lightning simulation discussed earlier. The main difference is that allowances must be made for the higher frequency content of the ESD event. That is to say that the parasitic parameters of capacitance, inductance, and transmission line effects must be modeled accurately. This procedure is best shown by example. The next section presents examples of both lightning and ESD event simulation at the system level.

Simulation Results

Lightning

Simulation of the FCC style lightning pulse is straightforward and is shown in Figure 7 along with the line of code describing the pulse source.



Ipulse 0 gen,
exp(0 750 .1us 4us 20us 240us 2000us)

Figure 7

In Figure 7, RPULSE is the typical output impedance of a lightning surge generator used to produce a longitudinal voltage surge. RPOUT represents the resistance from the telephone connections on a circuit pack to the backplane in the cabinet. The pulse generator used has a peak current of 750 Amps (yields 1500 volts across the 2 ohms of RPULSE). After a delay of .1 microsecond, the output increases from zero exponentially toward 750 amps with a time constant of 4 microseconds for 20 microseconds. At that point the current exponentially decays with a time constant of 240 microseconds for 2000 microseconds.

An important observation to make is that most voltage drops in a system caused by a lightning surge are due to L*di/dt, not the resistance of the conductors. Thus, one might expect the the maximum effect of the surge should be over after a few microseconds for our example.

Figure 8 contains a diagram of the first simulation example.

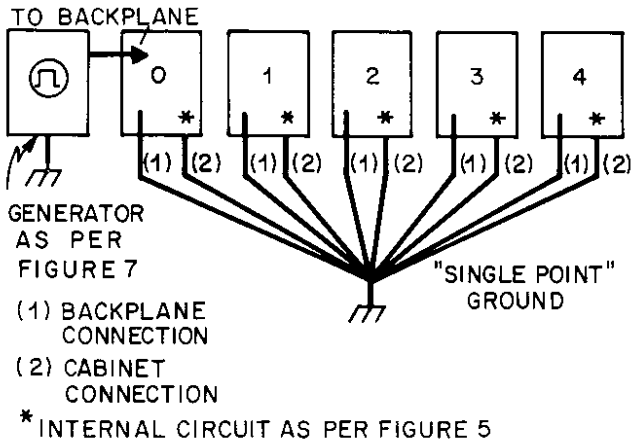


Figure 8

The lightning generator of Figure 7 is connected to a five cabinet PBX installation where the backplanes are grounded separately from the cabinets. The internal circuit model of each cabinet is shown in Figure 5. Each backplane and each cabinet are grounded through separate conductors to a "single point" ground. The surge is injected into the backplane of the first cabinet. This is not necessarily a recommended way to ground such a system, but it affords a good opportunity to show how a simulation such as this can help predict ground structure performance in a large system.

In the following simulation results I present voltage waveforms only. System voltages caused by lightning have safety and circuit damage implications. Currents can also become important, but in the interest of brevity I will address only voltages.

The voltage from cabinet 0 to the single point ground (SPG) is displayed in Figure 9 for the first 4 microseconds.

The peak voltage reaches about 22 volts and displays ringing from the tuned circuits. The general shape of the waveform is the L*di/dt drop in the ground paths.

Figure 10 plots the voltage between cabinets 0 and 1 and contains a surprise.

The voltage between cabinets 0 and 1 exceeds by a small amount the voltage from cabinet 0 to ground! The 1800 pF of intercabinet capacitance in combination with the ground wire inductances causes pronounced ringing.

This result is important for two reasons. First, any circuit in cabinet 0 that communicates over a metallic path with a circuit in cabinet 2 is likely to be stressed by something close to the intercabinet voltage unless special precautions are taken. Second, all the values assumed for parameters, such as

cabinet spacing and length of ground wires, are subject to wide variations in field installations. Therefore, the 24 volts peak between cabinets could be much larger than that for some installations, for instance, those with longer ground conductors or a combination of parameters that results in system ground resonances that match more closely the frequency content of the lightning surge.

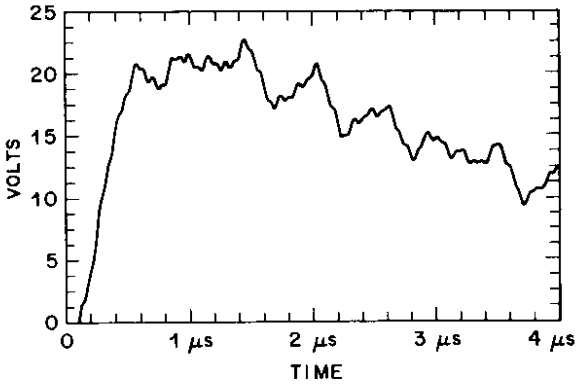


Figure 9

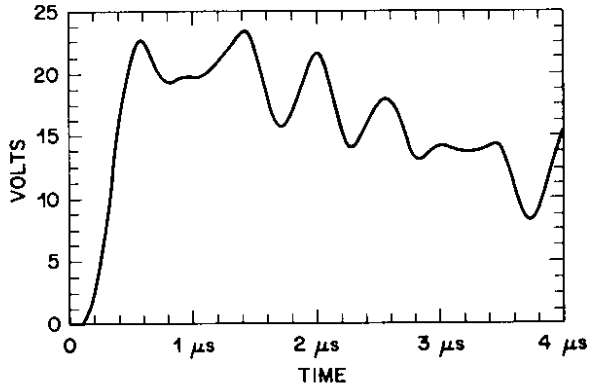


Figure 10

Figures 11 and 12 show waveforms corresponding to those in Figures 9 and 10 if the cabinets are bonded together with 50 nanohenries of inductance (a few inches of heavy wire).

The cabinet 0 to ground voltage has been reduced to about 6 volts because of the multiple paths to ground that now exist from cabinet 0. The ringing frequency has been increased and the ringing decays substantially over the 4 microseconds displayed. The cabinet 0 to cabinet 1 voltage (Figure 12) only reaches a peak of 0.4 volts. Circuits communicating between cabinets would be unlikely to be damaged by this arrangement.

A more economical installation is shown in Figure 13.

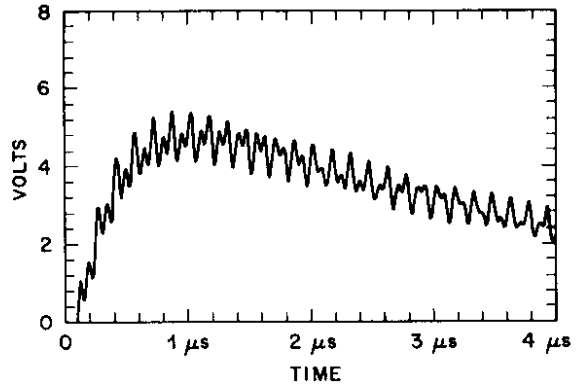


Figure 11

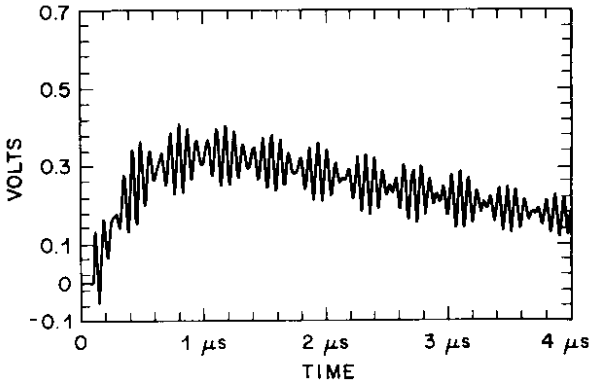


Figure 12

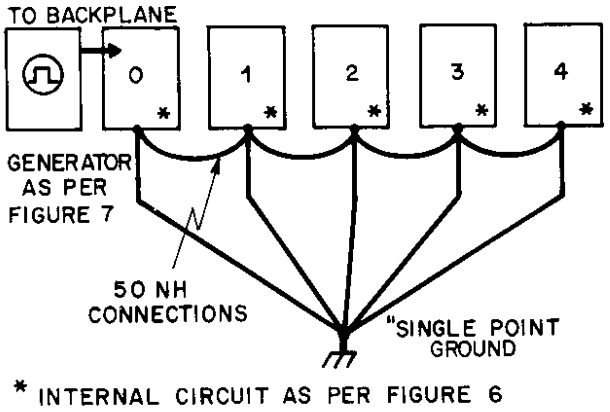


Figure 13

This involves connecting the backplanes internally to the cabinets through 100 nH conductors, bonding the cabinets together with 50 nH conductors, and separately grounding each cabinet. The internal circuit model for each cabinet is shown in Figure 6. As before, the surge is injected into the backplane of the first cabinet. Figures 14 and 15 display the cabinet 0 to ground and cabinet 0 to cabinet 1 voltages, respectively, for this case.

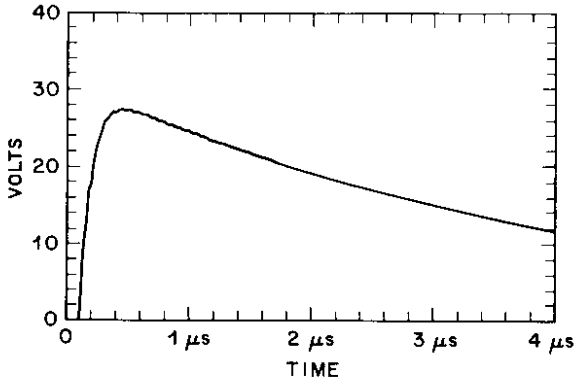


Figure 14

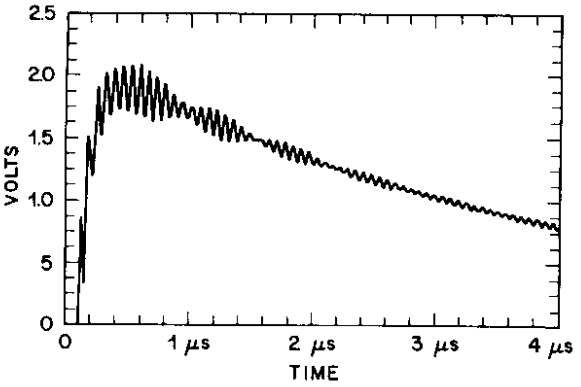


Figure 15

Figure 14 shows that cabinet 0 reaches about 27 volts peak to ground. However, Figure 15 shows that a cabinet 0 to cabinet 1 voltage of only 2 volts results. Thus, the simulation shows that low cabinet to cabinet voltage can be obtained without the need for separate ground wires from backplanes and cabinets.

Electrostatic Discharge

The performance of data processing and transmission equipment in the presence of ESD events is critical. Although damage prediction is important, ESD induced errors and recovery from those errors are issues that occur more frequently than damage in the field.

A simplified data transmission system between two pieces of computer equipment using twisted pair telephone wiring is shown in Figure 16. This example has been investigated under laboratory conditions and correlation established with ADVICE simulations.

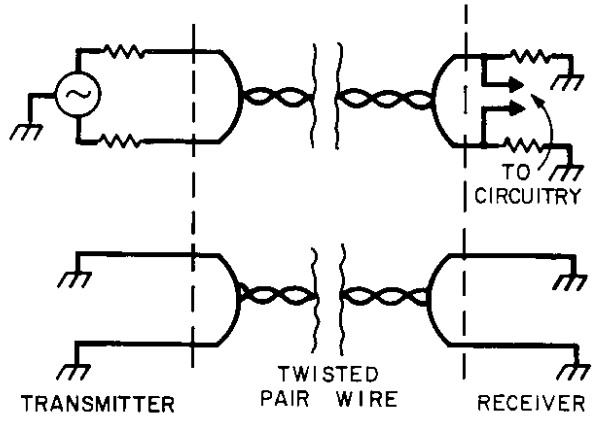


Figure 16

One pair of wires is used for the balanced signal and another is used to complete a ground connection between the two pieces of equipment. The problem occurs in that a discharge from an equipment operator on the transmitter may generate voltages on the data receiver input that exceed its common mode voltage range. Even though the voltage may not be enough to damage the receiver, corruption of the data is possible. Both possibilities must be investigated through simulation to ensure reliable operation. Simulating the system allows one to see the effect of changing parameters more quickly than may be the case in the lab. Configurations that are not able to be built in the laboratory environment can also be checked out.

To understand the problem to be simulated refer to the simplified diagram in Figure 17.

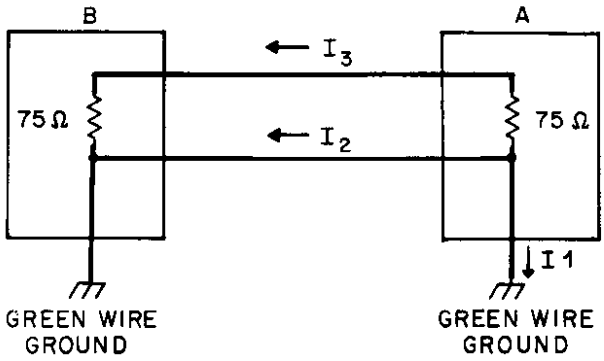


Figure 17

The diagram shows only one half of the balanced data circuit. During and after an ESD event the discharge current follows three paths out of equipment "A." Most of the discharge current flows out of the green wire ground conductor of the power cord to building ground (I1). Some current flows out though the ground conductor pair (I2) and the signal wire (I3) to equipment "B" and then to ground through its ground

connection. Current I3 can result in a voltage that exceeds the common mode voltage range of a data receiver powered from 5 volt power supplies. Current I3 flows because there is a difference of potential between equipment A and B. The total current flowing between them divides between I2 and I3.

One possible solution to ESD data corruption or damage is shown in the simplified diagram of Figure 18.

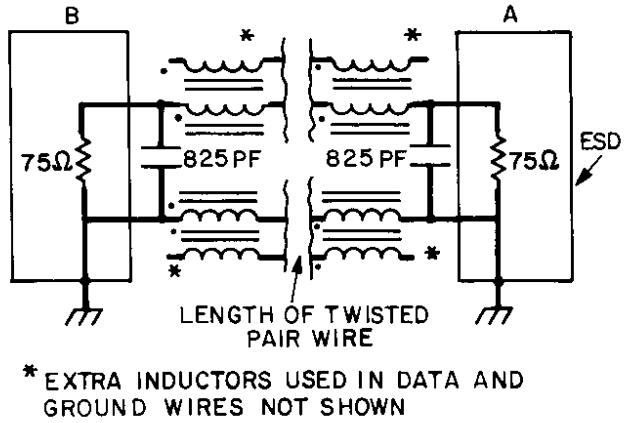


Figure 18

In this configuration all data wires and ground wires pass in common through one or more ferrite cores. These cores reduce the current flow and by inducing the drop across the ground circuit into the data circuit, reduce the common mode signal at the receiver caused by the ESD event. The small capacitors help in filtering out high frequency components.

Circuit models used for the ferrite cores and sections of wire connecting the data transmitter and receiver are shown in Figures 19 and 20 respectively.

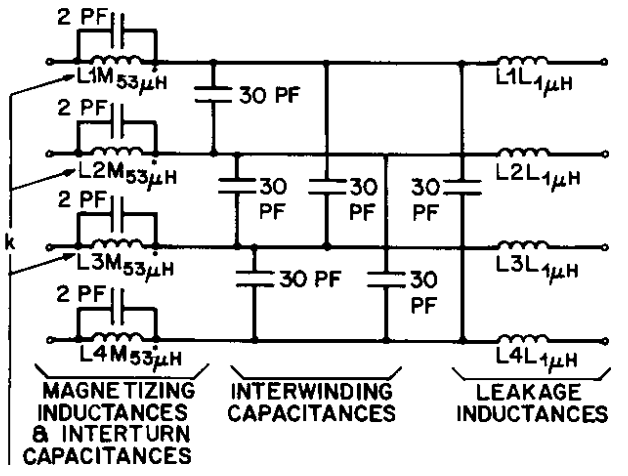


Figure 19

Due to the high frequency components present it is necessary to closely model as many parasitic parameters of the cores and cable as possible. For the ferrite core model it is important to model the interturn capacitances as well as the mutual inductances. These two parameters have a large effect on the results obtained.

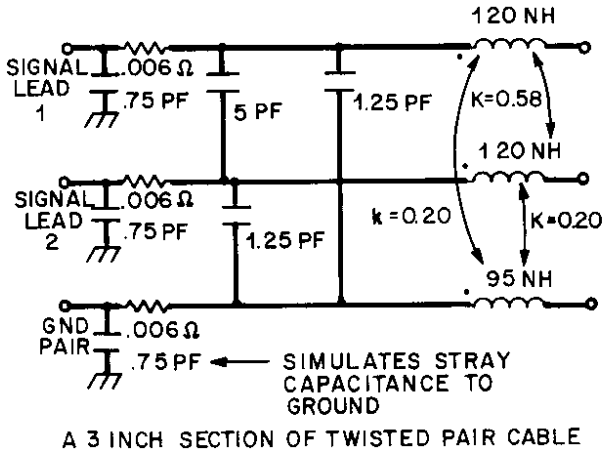


Figure 20

The cable model should include capacitance to ground from the wires. If it is left out, the analysis program will calculate a common mode transmission velocity of the ESD voltage will be much faster than possible. Since this parameter is difficult to measure in a real installation I recommend that a value be picked that yields reasonable transmission propagation speed for the ESD common mode voltage.

Figures 21 and 22 show the two configurations that I will now present simulation results for. In both of these cases the data equipment uses two coax cables to carry a balanced data signal and baluns are used to interface the data signals to the twisted pair wiring.

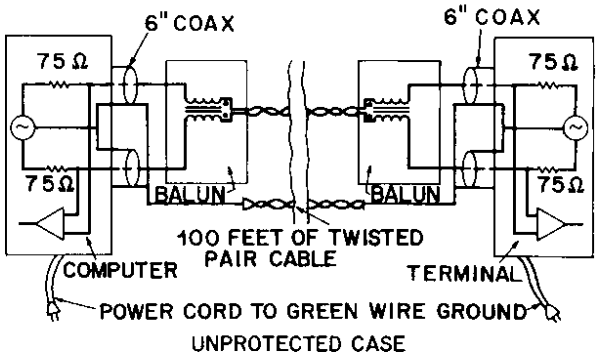


Figure 21

Figure 21 shows the standard data transmission case with no ESD protection. It is composed of the source and load impedances and the transmission media. In Figure 22, protection circuitry mainly composed of six ferrite cores with a relatively small number of turns on each core have been added on both ends of the transmission line. The series of cores reduces interturn capacitance of the windings in a fashion

similar to the way RF chokes are wound.

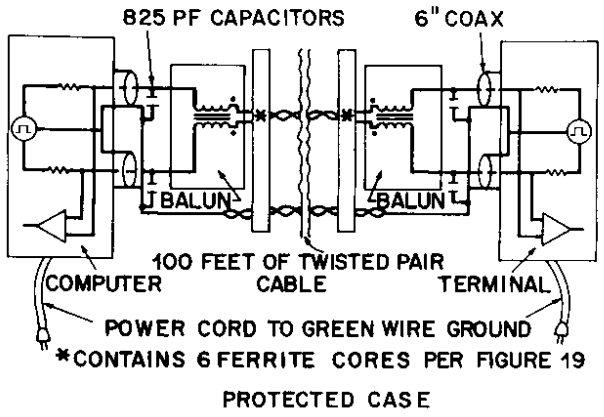


Figure 22

Unprotected Case

Figure 23 shows the output waveform impressed across the load resistor, Rx of Figure 21, because of a discharge to the data generator chassis.

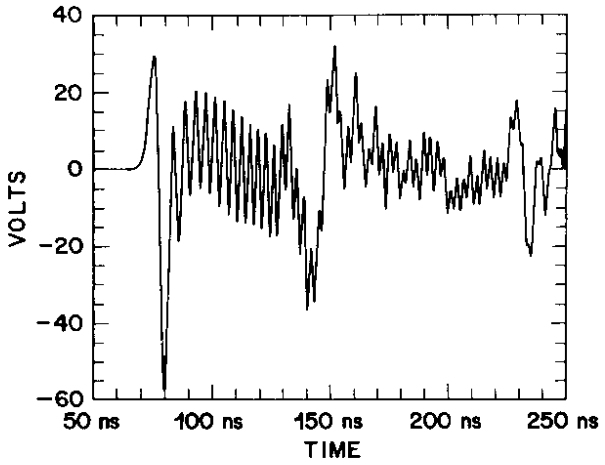


Figure 23

Note the excursions from +30 to almost -80 volts over the first 250 ns after the discharge. This waveform certainly exceeds the common mode range of 3 volts for input circuitry powered from 5 volt supplies. The timestep used for Figure 23 is 0.5ns.

Figure 24 shows the same waveform for a period of 1 microsecond using a 2 ns timestep.

Even though the waveform shape is close to that of Figure 23 for the first 250 ns, the amplitude is somewhat lower (+30 to -35 volts). This is caused by time constants in parts of the circuit that are faster than the timestep of 2 ns that was used. Some information from the plot is useful, though. I believe it is safe to say that Figure 24 shows that the waveform is not increasing over the 1 microsecond displayed.

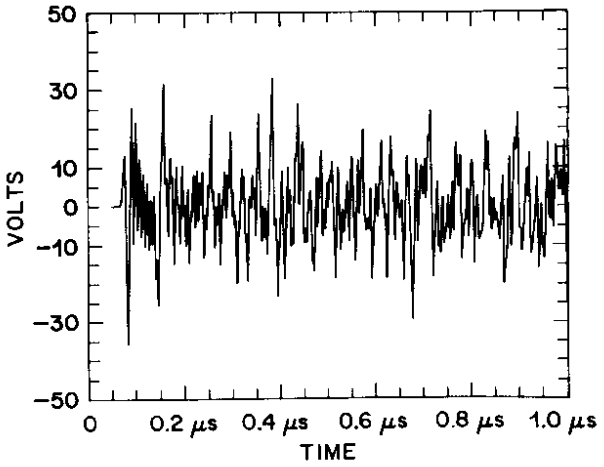


Figure 24

Protected Case

An advantage of simulation is that one can investigate configurations that are not necessarily realisable or practical but can be used to understand how various parameters contribute to the circuit response of an ESD event. I will now show how the various parameters of magnetizing inductance, mutual inductance, and the high frequency filter capacitance (825 pF capacitor in Figure 22) affect this example's ESD response.

Figure 25 shows the same case as Figure 23 except that the magnetizing inductances of the ferrite inductors of Figure 22 are added. There is no coupling between these inductors so this is not a useful data transmission arrangement. However, the waveform reaches a peak value of only 5 volts now, an improvement by a factor of 10 or so. The inductance has also produced new resonances.

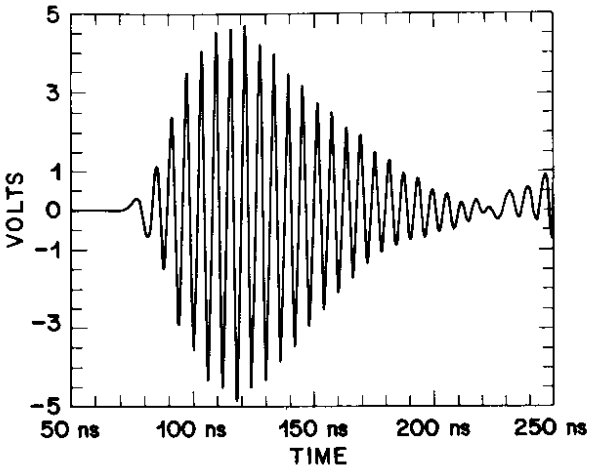


Figure 25

The waveform of Figure 25 is shown for one microsecond in Figure 26 with the timestep increased to 2 ns as in Figure 24.

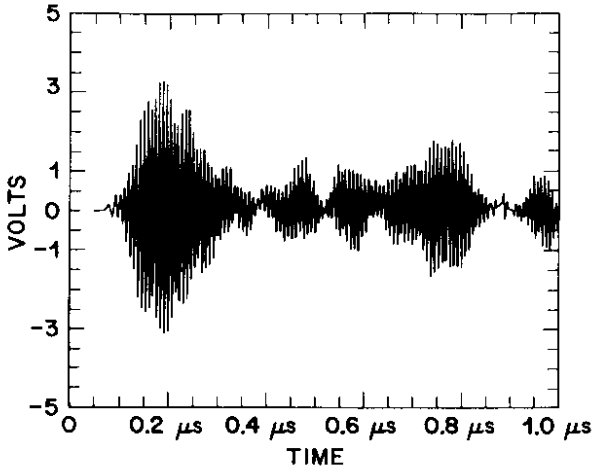


Figure 26

As in Figure 24, there is some amplitude error (+/- 3 volts peak instead of 5 volts) as well as some waveshape error over the first 250 ns because of the longer timestep. However, I believe this plot shows that the trend is toward lower amplitudes with time, i.e. there are no resonant frequencies much lower than those seen in the plot.

With mutual inductance added to the circuit, the result corresponding to Figure 25 is shown in Figure 27.

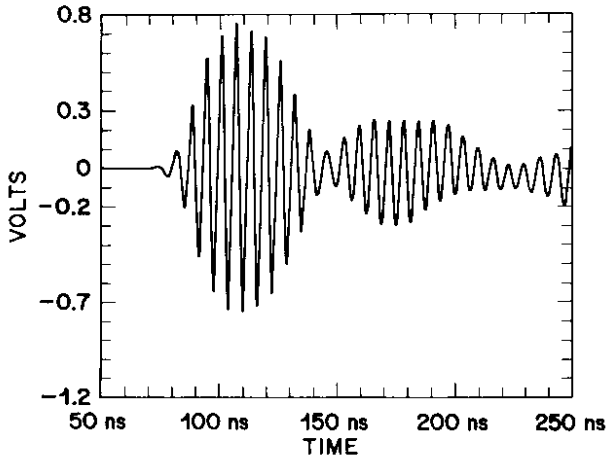


Figure 27

The amplitude is now less than one volt. Figure 28 shows the same output over one microsecond with a 2 ns timestep and with the same caveats and conclusions as before.

Figures 29 and 30 show the output waveform across the load with the high frequency capacitors of Figure 22 added (825pF) to the magnetizing and mutual inductances of the previous plots. To show that .5 ns is an adequate timestep, Figure 29 uses a .1 ns timestep and Figure 30 uses a .5 ns timestep. By using the largest possible timestep, more of a waveform can be plotted. Figure 29 only plots for the range of 80 to 110 ns compared to 50 to 250 ns for Figure 30.

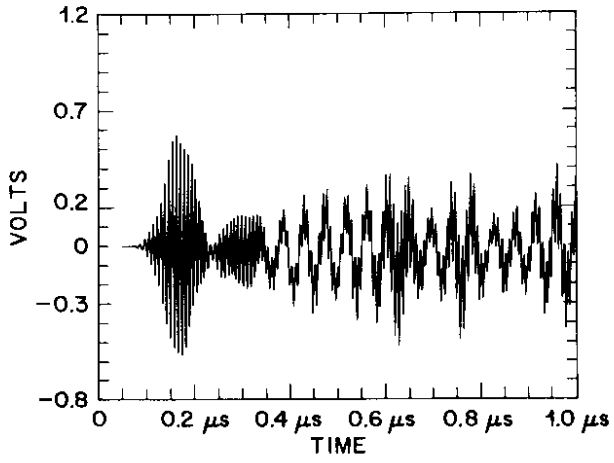


Figure 28

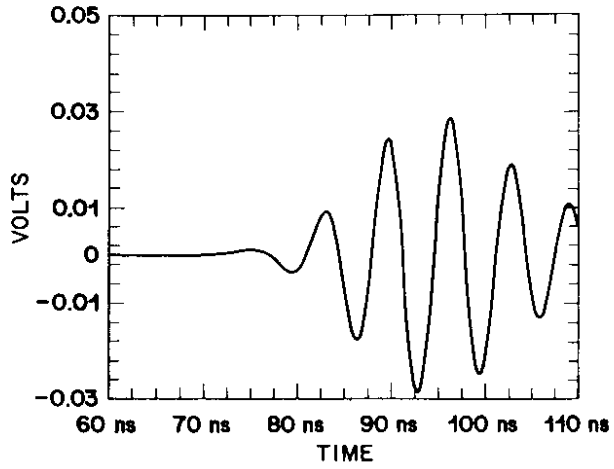


Figure 29

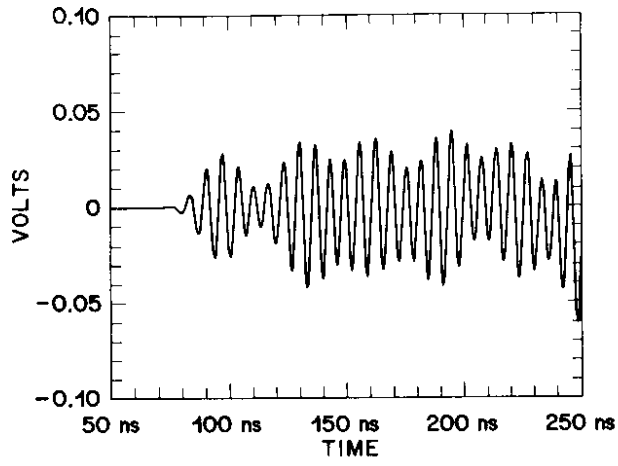


Figure 30

The part of Figure 30 that covers the same time range as Figure 29 agrees well with Figure 29. A lower frequency component just begins to show in Figure 30 so Figure 31 shows the waveform to .5 microsecond with a 1 ns timestep. The first part of Figure 31 shows some waveform distortion but the peak amplitude accuracy is good. Figure 31 does show a low frequency response that does need to be taken into account in designs. This low frequency component more than doubles the peak voltage across the load. Note, however, that with all the protection in place the peak voltage is now only about 0.1 volt. This represents almost a factor of 800 improvement over the unprotected design!

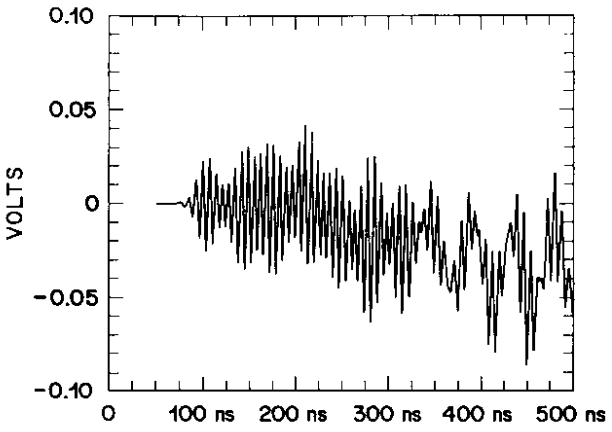


Figure 31

Figure 32 extends the range of Figure 31 to one microsecond using a 2 ns timestep. Compared to Figure 30, there is some amplitude and waveform distortion over the time common to both plots. The peak amplitude of the first few peaks of Figure 32 is only 25 volts compared to about 30 volts for Figure 30. However, Figure 32 does seem to show that the situation is no worse than that shown in Figure 31.

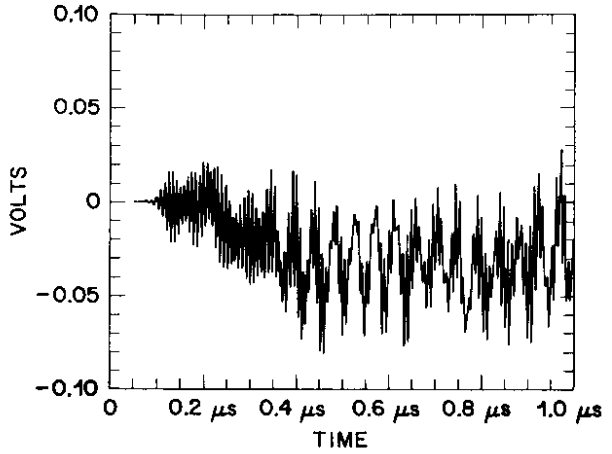


Figure 32

It is possible to compute with .1 ns timesteps and plot every 2 ns to maintain accuracy. However, many of these simulations can involve thousands of components after the subcircuits are expanded. Computation time can become an issue. The procedure I have followed in Figures 29 through 32 gives useful output with reasonable accuracy.

Summary

In this paper I have compared the modeling techniques for lightning and ESD simulation. The following points were discussed:

1. Modeling of the energy source:

   Standard waveforms for lighting and a model of an ESD generator using an ideal switch were presented.

2. Modeling of high frequency parasitics:

   Calculations involving inductance, inductive coupling, and capacitance were discussed. Parasitics that normally do not affect circuit operation can become important in lightning and ESD events.

3. Modeling of transmission lines:

   Lumped elements and nested subcircuits can reduce the effort required to simulate complex transmission lines.

4. Timestep considerations in ESD simulation:

   Circuit parasitic elements and the fast risetime of the ESD voltage contrast sharply with normal circuit operation that can be at much lower frequencies than ESD energy. This contrast creates large differences in the time constants of the circuit simulation. A procedure for determining an adequate timestep for simulation was presented.

These concepts were demonstrated with several examples from PBX and data transmission systems. For a data transmission system, circuit changes that resulted in an 800 fold improvement in ESD hardening were shown.

References

1. L. W. Nagel, "ADVICE for Circuit Simulation," Proc 1980 International Symposium on Circuits and Systems, Houston, Texas, April 28, 1980.

2. Tarak N. Bhar, Edward J. McMahon, "Electrostatic Discharge Control," Hayden Book Company, Inc., 1983, pp. 184--190.